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AMENDMENTS TO THE CLAIMS

Kindly amend claims 1, 6, 8-10, 12, 15, 22, 24-25, 28, 31-32, 36, 39, 45, and 48, and add new claims 51-70, as shown in the following listing of claims. The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (currently amended) A branch prediction apparatus in a processor including address selection logic for providing a fetch address to an instruction cache, the fetch address used to select lines of the instruction cache, the apparatus comprising:

first and second branch predictors, for providing first and second target address predictions of ~~an unconditional~~ branch instruction to the address selection logic;

instruction decode logic, configured to receive and decode said ~~unconditional~~ branch instruction and to generate a type thereof; and

branch control logic, configured to control the address selection logic to select said first prediction as the fetch address, said first prediction selecting a first line of the instruction cache;

wherein said branch control logic is further configured to subsequently selectively control the address selection logic, based on said branch instruction type, to select said second prediction as the fetch address, said second prediction selecting a second line of the instruction cache.

2. (original) The apparatus of claim 1, further comprising:

comparison logic, coupled to said first and second branch predictors, for comparing said first and second target address predictions.

3. (original) The apparatus of claim 2 wherein said type includes a specification of whether said branch instruction is a return type branch instruction.

4. (original) The apparatus of claim 3, wherein said branch control logic controls the address selection logic to select said second target address prediction if said branch instruction type is a return instruction and said first and second predictions miscompare.

5. (original) The apparatus of claim 4, wherein said second branch predictor comprises a call/return stack for providing said second target address prediction of said return instruction.

6. (currently amended) The apparatus of claim 2, wherein said type includes a specification of whether said ~~unconditional~~ branch instruction is a program counter-relative type branch instruction.